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vsim - continued

Key Arguments (use –help for full list)

[-restore <filename>]	Restore a simulation
[-sdf{min|typ|max} <region>=<sdffile>]	Apply SDF timing data e.g., sdfmin /top=MySDF.txt
[-sdfnowarn]	Disable SDF warnings
[-sv_seed <seed>]	Specify a seed for the Random Number Generator of the root thread
[-t [<mult>]<unit>]	Time resolution
[-vcdstim [<instance>=]<filename>]	Stimulate the top-level design or instances from an Extended VCD file
[-version]	Returns vsim version
[-vopt]	Run vopt automatically
[-novopt]	Disables automatic vopt run
[-voptargs="<args>"]	Arguments to pass to vopt
[-view <filename>]	Log file for VSIM to view
[-wlf <filename>]	Log file to create
[<libname>.<design_unit>	Configuration, Module, Entity/Arch, or optimized design to simulate
[-wlfcachesize]	Specify WLF reader cache size (per WLF file.)
[-wlfslim <size>]	Specify the number of Megabytes to be saved in event log file
[-wlftlim <duration>]	Specify the duration of time to be saved in event log file

Examples

vsim top

vsim -lib mywork top -do commands.do

qverilog

The qverilog command compiles, optimizes, and simulates Verilog and SystemVerilog designs in a single step.

1. automatic work library creation
2. support for all standard vlog arguments
3. support for C/C++ files via the SystemVerilog DPI
4. implicit "run -all; quit" unless using -i, -gui, -do (see -R below)
5. vopt peformance invoked (see the vopt section of this guide)

Key arguments to qverilog

<filename>	Verilog source code file to compile, one is required
[-R <sim_options>]	vsim command options applied to simulation

SVA & PSL

Key arguments to vcom and vlog

[-pslfile <file>]	External PSL file
[-nopsl]	Ignore embedded PSL assertions

Key arguments to vsim

[-nopsl]	ignore embedded PSL assertions
[-nosva]	ignore SystemVerilog concurrent assertions

Key Commands

assertion fail	Assertion failure response
assertion pass	Assertion pass response
assertion report	Assertion status report
fcover clear	Clear coverage meta-data
fcover	Adds meta-data to coverage database
fcover configure	Functional coverage target configuration
fcover report	Functional coverage results report
fcover save	Save data to reloadable file
vcover merge	Merge coverage data files offline

Key modelsim.ini variables

AssertionFail*	Control assertion failure behavior
AssertionFormat*	Define messages for VHDL assertion types
AssertionPass*	Control assertion pass behavior
BreakOnAssertion	Stop the simulator after assertion message
Cover*	Control cover directive behavior
IgnoreSVA*	Control SVA message logging
Sv_Seed	Seed random number generator

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Code Coverage

Key Arguments to vcom/vlog

-cover bcefsx	Specifies coverage type(s)

Key Arguments to vsim

-coverage	Enables statistics collection

Wave Window

add wave <item>	Wave specific signals/nets
add wave *	Wave signals/nets in scope
add wave -r /*	Wave all signals/nets in design
add wave abus(31:15)	Wave a slice of a bus
view wave	Display wave window
view wave -new	Display additional wave window
write wave	Print wave window to file
<left mouse button>	Select signal / Place cursor
<middle mouse button>	Zoom options
<right mouse button>	Context Menu
<ctrl-f>	Find next item
<tab> (go right)	Search forward for next edge
<shift-tab> (go left)	Search backward for next edge
i or + | o or -	Zoom in | Zoom out
f | l	Zoom full | Zoom Last

Key modelsim.ini variables

WLF*	Waveform management variables
WLFCacheSize	Change default or disable WLF file cache

Tcl/Tk

Environment Variable

MODELSIM_TCL

Online Documentation

Help->Tcl Help
Help->Tcl Syntax
Help->Tcl Man Pages
Help->Technotes->MTI_Widgets

Language Syntax

command arg1 arg2 arg3 ...

Language Syntax: Command

set <var> <value>
expr <math expression>
exec <ShellCommand>
info <option> <procedure name>
winfo <option> <window name>

Language Syntax: Procedures

proc *name {arglist} {body}*

```
proc diag {a b} {
set c [expr sqrt($a*$a + $b
return $c }
```

Language Syntax: Conditionals

if *{boolean} {bodytrue} else {bodyfalse}*

```
if {$now < 10000} {echo $now}
```

Language Syntax: Loops

while *{boolean} {body}*
foreach loopVar {valuelist} {cmdBody}
for {initial} {test} {final} {body}

Poking around in Tcl/Tk

info	Get info on a Tcl construct
info xx	Find out the args to *info*
winfo	Get info on Tk widgets
winfo xx	Find out args to *winfo*
winfo children .	Return the sub-widgets to simulator

Light blue highlight denotes SE-only features. *Light orange highlight denotes Questa-only features.*

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Environment Variables/Key Files

Environment Variables (see the "printenv" command)

LM_LICENSE_FILE	***Required***	Pathname of *license.dat* file or port@host
DOPATH	Optional	Search path for ".do" files
EDITOR	Optional	Specifies editor for "edit" cmd
MODELSIM	Optional	Pathname of *modelsim.ini* file
MODELSIM_TCL	Optional	path to optional graphical preference file
MODELSIM_PREFERENCES	Optional	Pathname to user interface preferences
MODEL_TECH	***Don't Set***	FOR INTERNAL USE ONLY
MGC_LOCATION_MAP	Optional	Used as "soft" path to find files
PLIOBJS	Optional	Used to load PLI object files
TMPDIR	Optional	Used by VSIM for temp space

Key Files

.modelsim	GUI preferences file
startup.do	Default name of macro executed after design is loaded; See "startup=" line in modelsim.ini
transcript	Default filename that the transcript window activity is saved to
vsim.wlf	Default name of simulation log file saved by VSIM

modelsim.ini

Copy modelsim.ini to current directory

Execute vmap -c

Loading order (stops after finding first file)

1. $MODELSIM environment variable
2. Current directory if $MODELSIM is not set
3. In */<install_dir>/modeltech/<platform>* directory
4. In */<install_dir>/modeltech* directory

For Detailed Information see:

the "Simulator Variables" appendix in the User's Manual

GUI shortcuts

F2 = toggle active pane/window
F3 = zoom active pane/window

Support

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Design optimization options

1. The VoptFlow modelsim.ini variable sets the default design optimization on (1) or off (0).
2. Optimized designs simulate faster, while non-optimized designs provide object visibility for debugging.
3. Use +acc with vopt or vsim -voptargs with +acc for selective design-object visibility during debugging.
4. Read "Optimizing Designs with vopt" in the User's Manual for additional information.

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Key Commands

Commands may be used in the following locations: (Sh)ell, (M)odelSim> prompt, or (V)SIM> prompt.
See Command Reference for complete command list and syntax.

vcom	Sh, M, V	VHDL Compiler (see below)
vdel	Sh, M, V	Deletes a design unit from a specific library
vdir	Sh, M, V	Lists the contents of a library
vlib	Sh, M, V	Creates a design library
vlog	Sh, M, V	Verilog Compiler (see below)
sccom	Sh, M, V	SystemC Compiler (see below)
vmap	Sh, M, V	Defines or displays library mappings
vopt	Sh, M, V	Optimize design (see *Performance* below)
vsim	Sh, M, V	Load design (see below)
qverilog	Sh,M, V	Single-step compile and simulate
add list / wave	V	Add signals to the List or Wave windows
add log	V	Log signals to *vsim.wlf* file for analysis later
alias	M, V	Create a user defined alias (e.g., *alias h "history"*)
bp, bd	V	Set/Clear a breakpoint
cd	Sh, M, V	Change directory
change	V	Modify a VHDL variable or Verilog register
checkpoint	V	Save the state of you simulation (see *restore*)
compare add	M, V	Compare signals
configure	M, V	Configure List or Wave window attributes
delete	V	Remove HDL item from List or Wave window
do	M, V	Execute a file of commands (e.g., *do macro.do*)
drivers	V	Display current and future value of signal or net drivers
dumplog64	Sh	Dump the contents of the *vsim.wlf* file in a readable form
echo	M, V	Display message (e.g., *echo "Time is $now ns."*)
edit	M, V	Invoke editor specified by the EDITOR env variable
environment	M, V	Display or change current region/signal environment
examine	M, V	Examine one or more HDL items (e.g., *exa /top/clk*)
find	V	Display pathnames of matching HDL items
force	V	Force signals or nets (e.g., *force clk 1 10, 0 20 -r 100*)
history	M, V	List previous commands
noforce	V	Release signals or nets from force commands
notepad	M, V	Simple text editor
printenv	M, V	Display names and values of environment variables
profile on	M, V	Turn on Performance Analyzer
property	V	Change List or Wave signal attributes (color, radix, etc.)
pwd	M, V	Display current path in Main transcript window
radix	M, V	Change the default radix in all windows
report	M, V	returns all control or state variable values
restart	V	Restart the simulator
restore	M, V	Restore the simulation state from a previous *checkpoint*
resume	M, V	Resume macro execution after a pause command
right / left	V	Search in wave window for next transition or -expr
run	V	Advance simulation time (e.g., *run 1000*)
search / next	V	Search specified window for next item matching pattern
seetime	V	Scroll List or Wave window to time (e.g., *seetime wave 500*)
vcd2wlf	Sh	Translate VCD file into WLF file
vcddumpports	M, V	Create a VCD file
vcover merge	Sh, M, V	Merges coverage reports
vgencomp	Sh	Create VHDL component from compiled Verilog module
view	M, V	Open a GUI window and pop it to the top
vmake	Sh	Print a makefile for a library
vsource	V	Display HDL source file in Source window
when	M, V	Perform action on condition (e.g., *when clk=1 {echo clk}*)
where	M, V	Display info about the environment
wlfman	Sh, M, V	manage waveform files
wlf2log	Sh, M, V	convert waveform file to log file
wlf2vcd	Sh, M, V	convert waveform file to vcd file
vcover	Sh, M, V	manage coverage information

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Key Commands - continued

Commands may be used in the following locations: (Sh)ell, (M)odelSim> prompt, or (V)SIM> prompt.
See Command Reference for complete command list and syntax.

write	M, V	Records names, window contents, and preferences to a file
!! | !n	M, V	Repeat last command, Repeat nth command
!abc	M, V	Repeat cmd starting "abc"
^abc^xyz	M, V	Replace "abc" in previous command with "xyz"

vlog

Key Arguments (use –help for full list)

[-vlog95compat]	Disable Verilog 2001 keywords
[-compat]	Disable event order optimizations
[-f <filename>]	Pass in arguments from file
[-hazards]	Enable run-time hazard checking
[-help]	Display *vlog* syntax help
[-nodebug]	Hide internal variables & structure
[-quiet]	Disable loading messages
[-R <simargs>]	Invoke VSIM after compile
[-refresh]	Regenerate lib to current version
[-sv]	Enables SystemVerilog keywords
[-version]	Returns vlog version
[-v <library_file>]	Specify Verilog source library
[-work <libname>]	Specify work library
<filename(s)>	Verilog file(s) to be compiled

Examples

```
vlog top.v
vlog –work mylib –refresh
```

vcom

Key Arguments (use –help for full list)

[-2002] [-93] [-87]	Choose VHDL 2002,1993, or 1987
[-check_synthesis]	Turn on synthesis checker
[-debugVA]	Print VITAL opt status
[-explicit]	Resolve ambiguous overloads
[-help]	Display *vcom* syntax help
[-f <filename>]	Pass in arguments from file
[-norangecheck]	Disable run time range checks
[-nodebug]	Hide internal variables & structure
[-novitalcheck]	Disable VITAL95 checking
[-nowarn <#>]	Disable individual warning msg
[-quiet]	Disable loading messages
[-refresh]	Regenerate library image
[-version]	Returns vcom version
[-work <libname>]	Specify *work* library
<filename(s)>	VHDL file(s) to be compiled

Examples

```
vcom  MyDesign.vhd
vcom  -93 -work /lib/mylib util.vhd
vcom  -refresh
```

Light blue highlight denotes SE-only features. *Light orange highlight denotes Questa-only features.*

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sccom

Key Arguments (use –help for full list)

-link	Links source code, required
[CPP option]	C++ compiler option
[-g]	Compile with debugging info
-vv	Echo subprocess invocations on stdout
[-scv]	Includes SystemC verification library
<filename(s)>	SystemC files to be compiled

Examples

```
sccom -g example.cpp
sccom -link example
sccom -I/home/systemc/include -g a.cpp b.cpp
```

vopt

Design optimization options

1. The VoptFlow modelsim.ini variable (below) sets the default design optimization on (1) or off (0).
2. Optimized designs simulate faster, while non-optimized designs provide object visibility for debugging.
3. Use +acc with vopt or vsim -voptargs with +acc for selective design object visibility during debugging.
4. Read "Optimizing Designs with vopt" in the User's Manual for additional information.

Key arguments to vopt

-o <name>	Optimized design name
<design>	Top-level design unit
[+acc=[<spec>]+[<module>]]	Enable design object visibility

Key arguments to vsim

[-vopt]	Run vopt if not automatically invoked
[-voptargs="<args>"]	Arguments passed to vopt, use +acc args for design visibility

modelsim.ini variable

VoptFlow = 1	Set vopt optimized flow as default
VoptFlow = 0	Set non-optimized flow as default

vsim

Key Arguments (use –help for full list)

[-0in]	Enable support for 0in tools
[-0in_options]	Specify options to be passed to the 0in tools in quotes
[-0in_voptflow]	Should be specified with -0in while loading a module optimized by vopt
[-assertdebug]	Keep data for debugging assertion failures
[-assertfile <filename>]	Alternative file for recording assert messages
[-assume]	Simulate PSL and Verilog assume directives same as assert directives
[-c]	Run in cmd line mode
[-coverage]	Invoke Code Coverage
[-do "cmd" | <file>]	Run cmd or file at startup
[-elab]	Create elaboration file
[-f <filename>]	Pass in args from file
[-gIG<name=value>]	Set VHDL Generic values
[-hazards]	Enable hazard checking
[-help]	Display vsim syntax help
[-l <logfile>]	Save transcript to log file
[-load_elab]	Simulate an elaboration file
[-noassume]	Do not simulate PSL and Verilog assume directives
[-nopsl]	Disable PSL assertions
[-nosva]	Disable System Verilog concurrent assertions
[+notimingchecks]	Disable timing checks
[-quiet]	Disable loading messages

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